UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,872	04/20/2004	Kenneth C. Creta	42P18867	5618

59796 7590 07/16/2007

INTEL CORPORATION
c/o INTELLEVATE, LLC
P.O. BOX 52050
MINNEAPOLIS, MN 55402

EXAMINER	
UNELUS, ERNEST	

ART UNIT	PAPER NUMBER
2181	

MAIL DATE	DELIVERY MODE
07/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/828,872	CRETA ET AL.	
	Examiner	Art Unit	
	Ernest Unelus	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO AMENDMENT

Claim rejections based on prior art

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/30/07 has been entered.

The instant application having Application No. 10/828,872 has a total of 36 preliminary amended claims pending in the application; there are 5 independent claim and 31 dependent claims, all of which are ready for examination by the examiner.

Applicant's arguments filed 04/30/2007, with respect to the rejection(s) of claim(s) 1-36 under Grun (US pat. 6,629,166) have been fully considered and is not persuasive. However, base on the amendment of the claims, upon further consideration, a new ground(s) of rejection is made in view of Grun (US pat. 6,629,166), Graham et al. (US pat. 6,223,641), and Kelly et al. (US pub. 2004/0019729).

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

4a. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4b. **Claims 1-6, 10-15, 19, 20, and 34-35,** are rejected under 35 U.S.C. 102(e) as being anticipated by Grun (US pat. 6,629,166).

5. As per **claims 1 and 34**, Grun discloses "A method comprising:

receiving from a processor a plurality of write transactions **(messages, as discloses in col. 7, lines 2-4)** write combine **(see col. 12, lines 10-11, which discloses "Each message primitive may contain a buffer ID field and a service contain a buffer ID field and a service contain a buffer ID field and a service connection ID field". As it known in the art, a**

message, request, command, or a data, is combine with addresses, such as source and destination addresses) in a processor **(see fig. 2, which discloses messages from the processor (initiator) 20 to the target channel adapter 22, see also col. 7, lines 1-13)**;

storing data associated with the plurality of write transactions in a buffer of an input/output (I/O) hub to form write combine data **(see fig. 3, which discloses buffering incoming messages and data into the 'message and data service' queue 30 that's inside the I/O hub 22 from the initiator; see col. 7, lines 33-52 for more detail)**; and

flushing **(to transmit, as it being interpreted by the examiner)** the write combined data associated with the plurality of write transactions to an I/O device according to a protocol between the I/O hub and the processor **(see fig. 3, which discloses transmitting data from the I/O hub 22 to an I/O controller within the target; see col. 7, lines 14-28)**.

6. As per **claims 2, 13, and 35**, Grun discloses "The method of claim 1," **[See rejection to claim 1 above]**, wherein flushing the data to the I/O device includes: determining whether a flush signal has been received from the processor **(col. 7, lines 52-55, discloses "The I/O controller 24, in turn, uses the services of the channel-based switched fabric to fulfill that request and to notify the initiator 20 that the request has been completed")**; and flushing the data if the flush signal has been received **(col. 7, lines 50-55, transmitting a receive signal (the flush signal) from the initiator)**, the protocol including an signaling protocol **(fig. 5 discloses a signaling protocol from the initiator)**.

7. As per **claims 3 and 14**, Grun further discloses "including sending a write completion signal to the processor for each of the write transactions before the data is flushed to the I/O device **(see fig. 6, which discloses sending a message signal to the I/O hub, which is first transfer to the I/O unit, then the data is flushed to the I/O device, see also col. 7, lines 14-28)**, each write completion signal verifying buffering of a corresponding write transaction **(see fig. 6, which discloses completion of a message)**.

8. As per **claims 4 and 15**, Grun further discloses "including sending a-flush completion signal to the processor after the data is flushed to the I/O device **(see fig. 5)**.

9. As per **claim 5**, Grun discloses "wherein flushing the data if the flush signal has been received further includes **(see fig. 6)**: tagging the buffer with a first source identifier **(the buffer ID, as discloses in col. 12, lines 10-15)** associated with one or more of the write transactions **(see col. 12, lines 10-15)**; detecting a second source identifier associated with the flushing signal **(the service connection ID, as discloses in col. 11 line 61 to col. 12, line 19)**; comparing the second source identifier to the first source identifier **(see col. 12, lines 10-11, which discloses "Each message primitive may contain a buffer ID field and a service connection ID". 'Comparing' is being interpreted by the examiner as to put side by side or together)**; and flushing the data to the I/O device if the second source identifier matches the first source identifier **(see fig. 6 and col. 11, line 61 to col. 12, line 4)**.

10. As per **claims 6 and 19**, Grun further discloses "including repeating the comparing for a

plurality of buffers **(see col. 12, lines 54-61, which discloses repeating the process for each request/command, which uses plurality buffers)**, each buffer corresponding to an I/O port **(fig. 3 shows multiple buffers corresponding to an I/O port)**.

11. As per **claims 10 and 20**, Grun discloses "wherein flushing the data to the I/O device includes flushing more than one cache line worth of data to the I/O device **(with respect to this limitation, page 1, paragraph 0003 from the applicant's specification discloses that a full cache line is about 64 byte. Similarly, Grun discloses data to the I/O device includes flushing more than one cache line worth of data to the I/O device. See col. 19, lines 17-32)**.

12. As per **claim 11**, Grun discloses "wherein the receiving includes receiving a plurality of commands instructing the I/O hub to consider each write transaction for write combining **(see col. 12, lines 20-33)**, each of the plurality of write transactions including one of the plurality of commands **(see col. 12, lines 30-33)**.

13. As per **claim 12**, Grun discloses "An input/output (I/O) hub **(target channel adapter 22 of fig. 2, which is further explain in fig. 3)** comprising:

receiving logic to receive a first and a second write transaction, the first and the second write transactions **(multiple messages, as discloses in col. 7, lines 2-4)** write combined **(see col. 12, lines 10-11, which discloses "Each message primitive may contain a buffer ID field and a service contain a buffer ID field and a service contain a buffer ID field and a service connection ID field". As it known in the art, a message, request, command, or a data, is**

combine with addresses, such as source and destination addresses) in a processor **(see fig. 2, which discloses messages from the processor (initiator) 20 to the target channel adapter 22, see also col. 7, lines 1-13),**

storage logic coupled to the receiving logic to store data associated with the first and second write transactions as write combined data **(see fig. 3, which discloses buffering incoming messages and data into the 'message and data service' queue 30 that's inside the I/O hub 22 from the initiator; see col. 7, lines 33-52 for more detail)** and

flushing logic coupled to the storage logic to flush the write combined data to an I/O device in response to a protocol event **(see fig. 3, which discloses transmitting data from the I/O hub 22 to an I/O controller within the target; see col. 7, lines 14-28).**

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. **Claims 7-9, 16-18, 31-33, and 36**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Grun (US pat. 6,629,166) in view of Graham et al. (US pat. 6,223,641).

16. As per **claims 7, 16, and 36**, Grun discloses "The method of claim 1," **[See rejection to claim 1 above]**, but fails to disclose expressly wherein flushing the data to the I/O device

includes: determining whether a latency condition exists; and flushing the data if the latency condition exists, the protocol including a timing protocol.

Graham discloses wherein flushing the data to the I/O device **(see col. 4, lines 34-42, which discloses transmitting data to I/O device 27a)** includes: determining whether a latency condition exists **(see col. 6, lines 52-57)**; and flushing the data if the latency condition exists **(see col. 6, lines 56-60)**, the protocol including a timing protocol **(see col. 10, lines 54-66)**.

Grun (US pat. 6,629,166) and Graham et al. (US pat. 6,223,641) are analogous art because they are from the same field of endeavor of a processor using an I/O hub to transmit data to an I/O device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a method for interfacing at least one Input/Output (I/O) controller to a channel-based switched fabric that includes: providing at least one channel adapter where the at least one channel adapter allows connection of the at least one I/O controller to a channel-based switched fabric and the at least one channel adapter supports transferring of messages and/or data between the at least one I/O controller and at least one initiating unit connected to the channel-based switched fabric; providing a physical interface between the at least one I/O controller and the at least one channel adapter; and defining a set of command primitives where the command primitives communicate information between the at least one I/O controller and the at least one channel adapter via the physical interface as described by Grun and a routing circuit that functions as a bridge between the primary bus and each of the first and second secondary busses, respectively, by associating each secondary bus with an address range, and forwarding a

command received from the primary bus to a secondary bus mapped to an address range including the address of the command as taught by Graham.

The motivation for doing so would have been because Graham teaches that " **the routing circuit directly routes to the second secondary bus, a command received from the first secondary bus addressed for the second secondary bus, without use of the primary bus. As a result, traffic and latency on the primary bus is reduced and efficiency is increased." (see col. 2, lines 38-44).**

Therefore, it would have been obvious to combine Graham et al. (US pat. 6,223,641) with Grun (US pat. 6,629,166) for the benefit of creating the method to obtain the invention as specified in claims 7, 16 and 36.

17. As per **claims 8 and 17**, the combination of Grun and Graham discloses "The method of claim 7," **[See rejection to claim 7 above]**, Grun further discloses including sending a write completion signal to the processor for each of the write transactions as the data is flushed to the I/O device **(see fig. 5)**, each write completion signal verifying flushing of a corresponding write transaction **(see fig. 6, which discloses the verification of a completion)**.

18. As per **claims 9 and 18**, the combination of Grun and Graham discloses "The method of claim 7," **[See rejection to claim 7 above]**, Grun further discloses "wherein the latency condition includes a delay in receiving a next combinable write transaction from the processor and an interface to the I/O device being in an idle state **(see fig. 11 and see col. 27, lines 9-15)**.

19. As per **claim 31**, Grun discloses "A method comprising:

receiving a plurality of write transactions from a processor **(messages, as discloses in col. 7, lines 2-4)**, the plurality of write transactions being destined for an input/output (I/O) device **(see fig. 2, which discloses the messages going to an I/O controller 24)**;

storing data associated with the plurality of write transactions to a buffer of the I/O hub **(see fig. 3, which discloses buffering incoming data inside the I/O hub 22 from the initiator, which also discloses transmitting data from the I/O hub 22 to an I/O controller within the target. see col. 7, lines 28-52)**; the latency condition including a delay in receiving a next combinable write transaction from the processor and an interface to the I/O device being in an idle state **(see fig. 11 and see col. 27, lines 9-15)**;

flushing the data to the I/O device if the latency condition exists **(see fig. 6)**; and sending a write completion signal to the processor for each of the plurality of write transactions as the data is flushed to the I/O device **(see fig. 5)**, each write completion signal verifying flushing of a corresponding write transaction **(see fig. 6, which discloses the verification of a completion)**.

but fails to disclose expressly wherein flushing the data to the I/O device includes: determining whether a latency condition exists; and flushing the data if the latency condition exists, the protocol including a timing protocol.

Graham discloses wherein flushing the data to the I/O device **(see col. 4, lines 34-42, which discloses transmitting data to I/O device 27a)** includes: determining whether a latency condition exists **(see col. 6, lines 52-57)**; and flushing the data if the latency condition exists **(see col. 6, lines 56-60)**, the protocol including a timing protocol **(see col. 10, lines 54-66)**.

Grun (US pat. 6,629,166) and Graham et al. (US pat. 6,223,641) are analogous art because they are from the same field of endeavor of a processor using an I/O hub to transmit data to an I/O device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a method for interfacing at least one Input/Output (I/O) controller to a channel-based switched fabric that includes: providing at least one channel adapter where the at least one channel adapter allows connection of the at least one I/O controller to a channel-based switched fabric and the at least one channel adapter supports transferring of messages and/or data between the at least one I/O controller and at least one initiating unit connected to the channel-based switched fabric; providing a physical interface between the at least one I/O controller and the at least one channel adapter; and defining a set of command primitives where the command primitives communicate information between the at least one I/O controller and the at least one channel adapter via the physical interface as described by Grun and a routing circuit that functions as a bridge between the primary bus and each of the first and second secondary busses, respectively, by associating each secondary bus with an address range, and forwarding a command received from the primary bus to a secondary bus mapped to an address range including the address of the command as taught by Graham.

The motivation for doing so would have been because Graham teaches that " **the routing circuit directly routes to the second secondary bus, a command received from the first secondary bus addressed for the second secondary bus, without use of the primary bus. As a result, traffic and latency on the primary bus is reduced and efficiency is increased." (see col. 2, lines 38-44).**

Therefore, it would have been obvious to combine Graham et al. (US pat. 6,223,641) with Grun (US pat. 6,629,166) for the benefit of creating the method to obtain the invention as specified in claim 31.

20. As per **claim 32**, the combination of Grun and Graham discloses "The method of claim 31," **[See rejection to claim 31 above]**, Grun further discloses "wherein flushing the data to the I/O device includes flushing more than one cache line worth of data to the I/O device **(with respect to this limitation, page 1, paragraph 0003 from the applicant's specification discloses that a full cache line is about 64 byte. Similarly, Grun discloses data to the I/O device includes flushing more than one cache line worth of data to the I/O device. See col. 19, lines 17-32)**.

21. As per **claim 33**, the combination of Grun and Graham discloses "The method of claim 31," **[See rejection to claim 31 above]**, Grun further discloses "wherein the receiving includes receiving a plurality of commands instructing the I/O hub to consider each write transaction for write combining **(see col. 12, lines 20-33)**, each of the plurality of write transactions including one of the plurality of commands **(see col. 12, lines 30-33)**.

22. **Claims 21- 30**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Grun (US pat. 6,629,166) in view of Kelly et al. (US pub. 2004/0019729).

23. As per **claim 21**, Grun discloses "A system comprising:

an input/output (I/O) device **(I/O target 24 in fig. 2, which includes the I/O controller)**;

a peripheral components interconnect (PCI) express bus coupled to the I/O device **(see fig. 1 and col. 1, lines 26-30)**; a processor **(see fig. 1)**; and

a chipset **(the channel-based switched fabric 16 in fig. 2)** having an I/O hub **(target channel adapter 22 in fig. 2, which is further explain in fig. 3)** coupled to the PCI express bus and the processor **(see fig. 2)**, the I/O hub having a buffer and a write combining module **(the target channel adaptor 22) (see col. 12, lines 10-11, which discloses "Each message primitive may contain a buffer ID field and a service contain a buffer ID field and a service contain a buffer ID field and a service connection ID field". As it known in the art, a message, request, command, or a data, is combine with addresses, such as source and destination addresses)** to receive a plurality of write transactions from the processor **(see fig. 3, which discloses buffering incoming messages and data into the 'message and data service' queue 30 that's inside the I/O hub 22 from the initiator; see col. 7, lines 33-52 for more detail). See also fig. 2, which discloses write transaction from the processor (initiator) 20 to the I/O hub 22, see also col. 7, lines 1-13)**, to store data associated with the plurality of write transactions in the buffer to form a write combined data set and **(see fig. 3, which discloses buffering incoming data inside the I/O hub 22 from the initiator, which also discloses transmitting data from the I/O hub 22 to an I/O controller within the target)** and to flush the write combined data set to the I/O device in response to event associated with the processor **(see fig. 3, which discloses transmitting data from the I/O hub 22 to an I/O controller within the target; see col. 7, lines 14-28)**, the data to be longer than one cache line**(with respect to this limitation, page 1, paragraph 0003 from the applicant's specification discloses that a full**

cache line is about 64 byte. Similarly, Grun discloses data to the I/O device includes flushing more than one cache line worth of data to the I/O device. See col. 19, lines 17-32)

but fails to disclose expressly wherein the PCI bus is a PCI Express bus.

Kelly discloses wherein the PCI bus is a PCI Express bus **(see paragraph 0003).**

Grun (US pat. 6,629,166) and Kelly et al. (US pub. 2004/0019729) are analogous art because they are from the same field of endeavor of a processor using an I/O hub (a bridge or switch) to transmit data to an I/O device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a method for interfacing at least one Input/Output (I/O) controller to a channel-based switched fabric that includes: providing at least one channel adapter where the at least one channel adapter allows connection of the at least one I/O controller to a channel-based switched fabric and the at least one channel adapter supports transferring of messages and/or data between the at least one I/O controller and at least one initiating unit connected to the channel-based switched fabric; providing a physical interface between the at least one I/O controller and the at least one channel adapter; and defining a set of command primitives where the command primitives communicate information between the at least one I/O controller and the at least one channel adapter via the physical interface as described by Grun and A method and implementing computer system are provided which allow for much improved input/output (I/O) subsystem designs for use in serialized I/o transaction systems including Express systems as taught by Kelly.

The motivation for doing so would have been because Kelly teaches that " **This invention defines means to greatly improve Express design requirements, making the design of Express devices such as an Express switch, Express-PCI bridge, endpoint, or root complex more efficient, less complex and therefore less costly" (see paragraph 0005).**

Therefore, it would have been obvious to combine Kelly et al. (US pub. 2004/0019729) with Grun (US pat. 6,629,166) for the benefit of creating the system to obtain the invention as specified in claim 21.

24. As per **claim 22**, the combination of Grun and Kelly discloses "The system of claim 21," **[See rejection to claim 7 above]**, Grun further discloses wherein the protocol event includes a flush signal from the processor **(col. 7, lines 52-55, discloses "The I/O controller 24, in turn, uses the services of the channel-based switched fabric to fulfill that request and to notify the initiator 20 that the request has been completed").**

25. As per **claim 23**, the combination of Grun and Kelly discloses "The system of claim 22," **[See rejection to claim 22 above]**, Grun further discloses wherein the processor is to generate the flushing signal if a flushing event has occurred and a write combine history indicates that one or more combinable write transactions have been issued by the processor **(see fig. 11)**.

26. As per **claims 24 and 25**, the combination of Grun and Kelly discloses "The system of claim 23," **[See rejection to claim 23 above]**, Grun further discloses wherein the write combine

history is to track combinable write transactions for a particular processor thread and an I/O hub **(see col. 12, lines 20-44)**.

27. As per **claim 26**, the combination of Grun and Kelly discloses "The system of claim 22," **[See rejection to claim 22 above]**, Grun further discloses wherein the chipset **(the channel-based switched fabric 16 in fig. 2)** includes a plurality of I/O hubs **(target channel adapter 22 in fig. 2 and host channel adapter 18 in fig. 2, which is further explain in fig. 3)**, the processor to send the flushing signal to each of the plurality of I/O hubs **(see fig. 2 and col. 6, line 60 to col. 7, line 13)**.

28. As per **claim 27**, the combination of Grun and Kelly discloses "The system of claim 26," **[See rejection to claim 26 above]**, Grun further discloses wherein the processor is to verify that one or more combinable write transactions have been sent to each of the plurality of I/O hubs before sending the flushing signal **(see fig. 6)**.

29. As per **claim 28**, the combination of Grun and Kelly discloses "The system of claim 21," **[See rejection to claim 21 above]**, Grun further discloses wherein the protocol event includes a latency condition **(see fig. 11 and see col. 27, lines 9-15)**.

30. As per **claim 29**, the combination of Grun and Kelly discloses "The system of claim 21," **[See rejection to claim 21 above]**, further discloses wherein the processor is to instruct the I/O hub to consider each write transaction for write combining based on a page table attribute

associated with the write transactions **(see paragraph 0043 of Kelly and col. 13, lines 26-56 of Gun)**.

31. As per **claim 30**, the combination of Grun and Kelly discloses "The system of claim 21," **[See rejection to claim 21 above]**, further discloses "including a point-to-point network interconnect coupled to the processor and the I/O hub **(see fig. Which discloses point–to-point topology, see also col. 8, lines 13-18)**, the network interconnect having a layered communication protocol **(see col. 7, lines 9-12)**.

RELEVANT ART CITED BY THE EXAMINER

32. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

33. The following reference teaches write transactions on an input/output (I/O) hub according to a protocol between the target and a processor.

U.S. PATENT NUMBER

US 2004/0193757

US 2005/0066225

US 2002/0174229

US 2005/0005044

CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

34. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

35. Per the instant office action, claims 1-36 have received a first action on the merits and are subject of a first action non-final.

DIRECTION OF FUTURE CORRESPONDENCES

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ernest Unelus whose telephone number is (571) 272-8596. The examiner can normally be reached on Monday to Friday 9:00 AM to 5:00 PM.

IMPORTANT NOTE

37. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Alford Kindred, can be reached at the following telephone number: Area Code (571) 272-4037.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PMR system, see her//pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217- 91 97 (toll-free).

July 05, 2007

Ernest Unelus
Patent Examiner
Art Unit 2181

ALFORD KINDRED
PRIMARY EXAMINER